

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:
Masahiro Ishida et al.

Application No.: 10/779,904

Confirmation No.: 9608

Filed: February 17, 2004

Art Unit: 2136

For: METHOD AND APPARATUS FOR DEFECT
ANALYSIS OF SEMICONDUCTOR
INTEGRATED CIRCUIT

Examiner: Not Yet Assigned

SUBMISSION ACCOMPANYING REQUEST FOR CONTINUED EXAMINATION

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

In response to the Office Action dated January 31, 2008, please reconsider this application in view of the following.